

KYNESIS – POLARFIRE RISC-V

HW MANUAL



REVISION HISTORY

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CHAPTER 1

1. INTRODUCTION

This Chapter gives background information on this document.

Section includes :

- **Acronyms and Abbreviations Used**
- **Signal Table Terminology**
- **Document and Standard References**



This document is created to guide users design Kynesis compliant carrier board. It will focus only on the interfaces in Kynesis pinout and related peripherals.

This document also contains reference schematics for different interfaces.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

An evaluation carrier is available for Kynesis module.

1.1 ACRONYMS AND ABBREVIATIONS USED

The table below shows the acronyms and abbreviations used in the manual.

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX f is able to detect whether RX and TX need to be crossed (MDI or MDIX)
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor
DSI	Display Serial Interface
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDA	High Definition Audio (HD Audio), digital audio interface between CPU and audio codec
HDMI	High-Definition Multimedia Interface, combines audio and video signal
I2C	Inter-Integrated Circuit, two wire interfaces for connecting low speed peripherals
I2S	Integrated Interchain Sound, serial bus for connecting PCM audio data between two devices
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signalling, electrical interface standard that can transport very high speed signals over twisted-pair cables.
MSB	Most Significant Bit
NA	Not Available
NC	Not Connected
OD	Open Drain
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SOC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

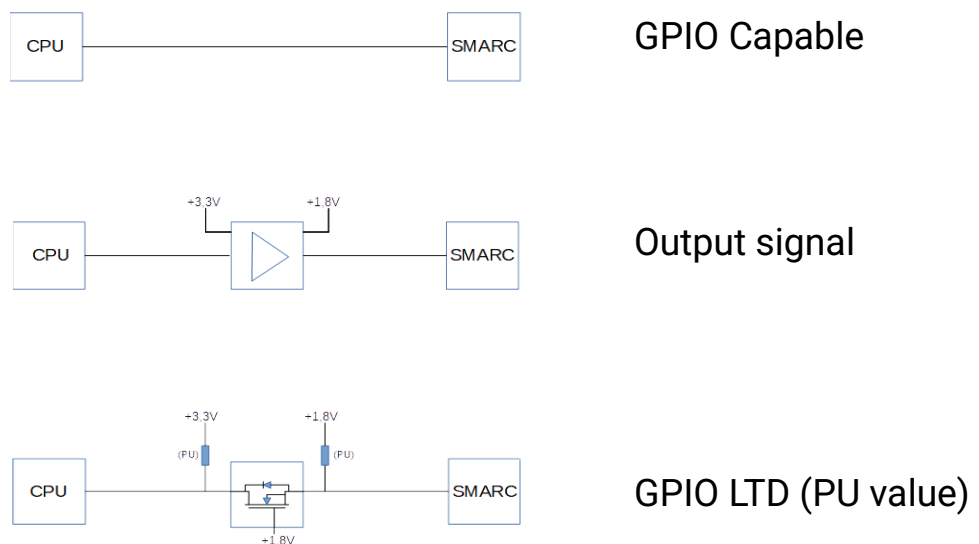
1.2 SIGNAL TABLE TERMINOLOGY

The Table below describes the terminology used in this section for the Signal Description tables.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

DIRECTION	TYPE	NOTE
Input		Input to the Module
Output		Output from the Module
Output OD		Open drain output from the Module
Bi-Dir		Bi-directional signal (can be input or output)
Bi-Dir OD		Bi-directional signal; output from the Module is open drain
Diff100		Differential 100 Ohm
Diff90		Differential 90 Ohm
	VDD_IN	Module input voltage
	CMOS 1.8V	CMOS logic input and / or output, 1.8V I/O supply level or tolerance
	CMOS 3.3V	CMOS logic input and / or output, 3.3V I/O supply level or tolerance
	CMOS VDD_IO	CMOS logic I/O level
	GBE MDI	Differential analog signalling for Gigabit Media Dependent Interface

Schematics reference for GPIO configurations and level translation



1.3 DOCUMENT AND STANDARD REFERENCES

1.3.1 EXTERNAL INDUSTRY STANDARD DOCUMENTS

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- PICMG® EEPROM Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org).
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- SPI Bus – “Serial Peripheral Interface” - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- USB Specifications (www.usb.org).

1.4 NON-INTENDED USE

WARNING

Use the Kynesis module in the specified temperature ranges only!

Use the Kynesis module in the specified humidity ranges only!

1.5 ELECTROSTATIC SENSITIVE DEVICE

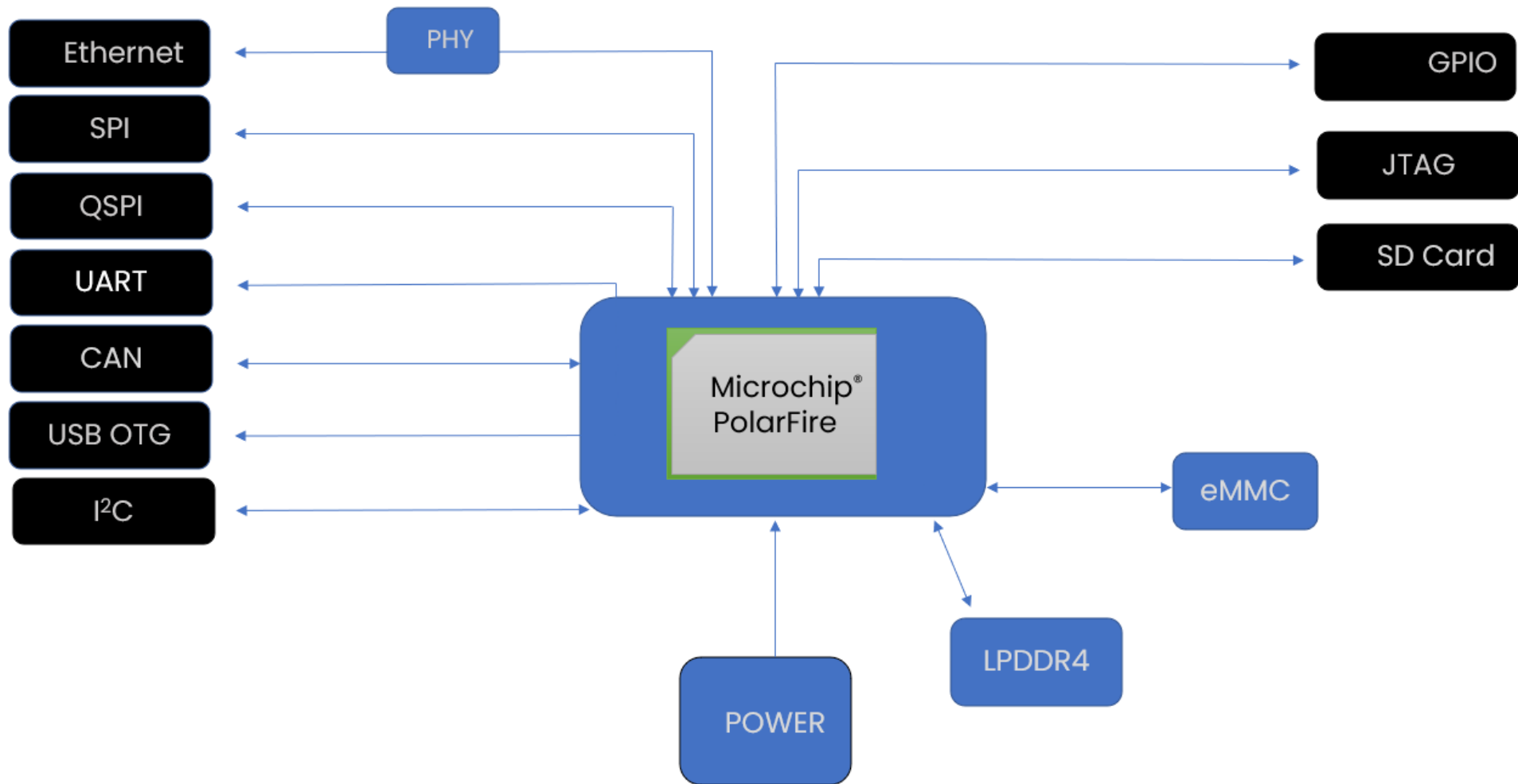
The ENGICAM Kynesis module is an electrostatic sensitive device and it is packed accordingly.

Warning:

Handle the Kynesis Module at electrostatic-free workstations only.

Do not handle or store the Kynesis Module near strong electrostatic, electromagnetic, magnetic or radioactive fields unless the Kynesis Module is contained within its original packaging.

1.6 BLOCK DIAGRAM



CHAPTER 2

2. ORDERING INFORMATION

This Chapter gives the ordering information and technical specifications of the modules.

Section includes :

- **Ordering code**
- **CPU & Memory specifications**
- **Operating temperature range**

2.1 ORDERING INFORMATION

Following is provided the ordering information and the description of the basic technical specifications for the modules:

Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU) ²⁾	Module available at least until ¹⁾
K026800011C550	1	Kynesis MPF025 (Microchip Polarfire MPFS025T-FCVG484E; Polarfire SOC, 2GB LPDDR4, 8GB eMMC, Extended temperature)	Microchip Kynesis MPFS025T-FCVG484E; Polarfire SOC, 2GB LPDDR4, 8GB eMMC	-10 to +85	4 th Q - 2034
K026700011C550	58			-10 to +85	4 th Q - 2034
K026800011I550	1	Kynesis MPF025 Industrial (Microchip Polarfire MPFS025T-FCVG484I; Polarfire SOC, 2GB LPDDR4, 8GB eMMC, industrial)	Microchip Kynesis MPFS025T-FCVG484I; Polarfire SOC, 2GB LPDDR4, 8GB eMMC	-10 to +85	4 th Q - 2034
K026700011I550	58			-10 to +85	4 th Q - 2034
K026800012C550	1	Kynesis MPF095 (Microchip Polarfire MPFS095T-FCVG484E; Polarfire SOC, 2GB LPDDR4, 8GB eMMC, Extended temperature)	Microchip Kynesis MPFS095T-FCVG484E; Polarfire SOC, 2GB LPDDR4, 8GB eMMC	-10 to +85	4 th Q - 2034
K026700012C550	58			-10 to +85	4 th Q - 2034
K026800012I550	1	Kynesis MPF095 Industrial (Microchip Polarfire MPFS095T-FCVG484I; Polarfire SOC, 2GB LPDDR4, 8GB eMMC, industrial)	Microchip Kynesis MPFS095T-FCVG484I; Polarfire SOC, 2GB LPDDR4, 8GB eMMC	-10 to +85	4 th Q - 2034
K026700012I550	58			-10 to +85	4 th Q - 2034

Startekits/Options		
K026K00012C550	Kynesis MPF095 Starterkit	Kynesis MPF095 module, evaluation board, USB power supply cable
K026K00012I550	Kynesis MPF095 Starterkit Industrial	Kynesis MPF095 Industrial module, evaluation board, USB power supply cable

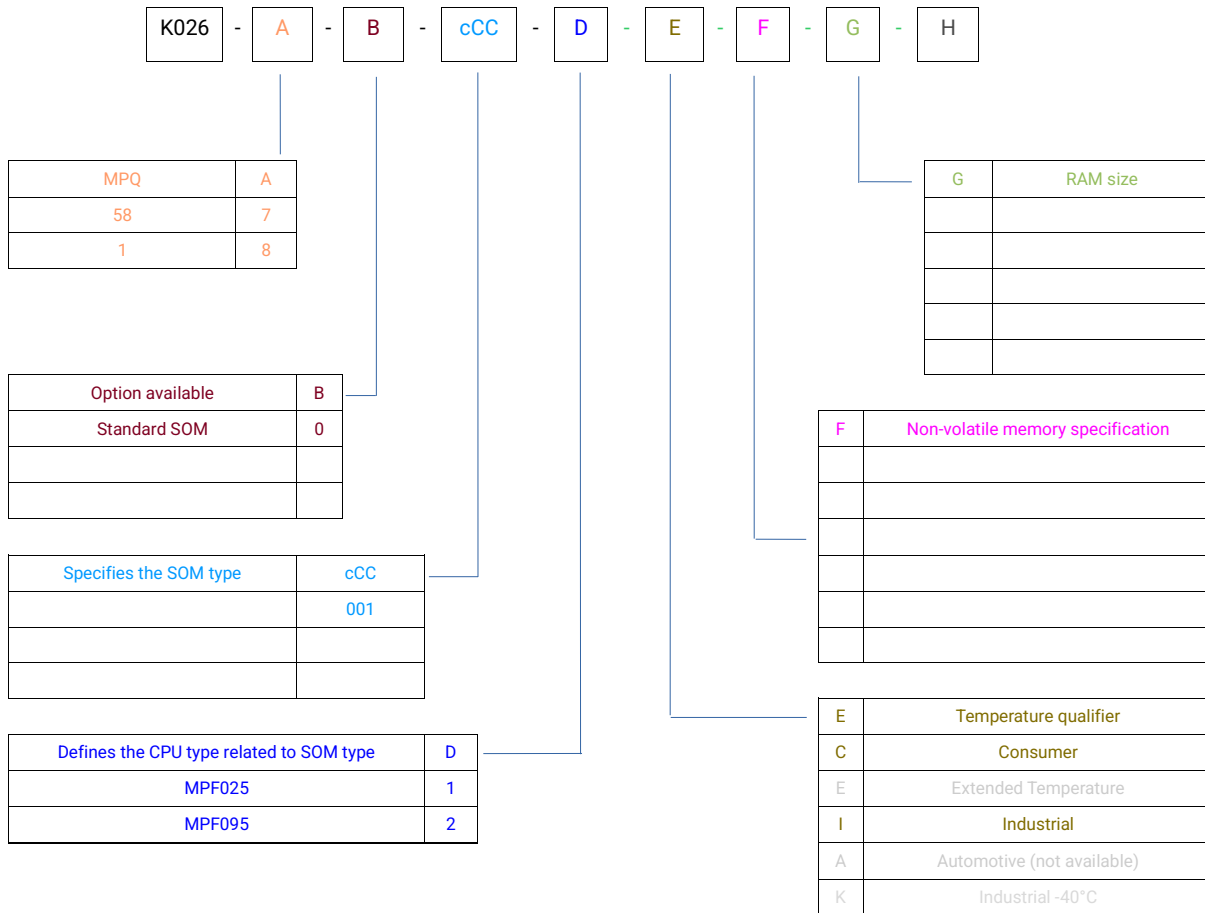
WARNING: the temperature depends on the application, the enclosure and/or the environmental condition. Upon customer to consider specific cooling solutions for its own final syst

¹⁾ Long Term Availability based on Microchip® longevity program

²⁾ Note: Internal junction temperature (Temperature Range T_J - Industrial SKUs: -40°C to 100°C – Extended commercial SKUs: 0°C to 100°C)

2.2 PART NUMBER STRUCTURE

The module is available with eMMC option. The standard order codes shown in the tables above shall be modified as follows:



WARNING: not all the custom configurations might be available in respect of standard time and orderable quantities

CHAPTER 3

3. PINOUT AND FEATURES

Section includes :

- **Pinout overview**

3.1 MODULE PINOUT

There are 260 edge fingers of the module that mate with a low profile 260 DDR4 Sodimm4 pitch0.5mm right angle connector
The SOM mates with connector TE 2309409-2 and compatible connectors

The following table lists the module pin assignments for all 260 edge fingers.

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
1	+3V3_ETH	Out Power Pin					2	GND					
3	GND	Power PIN					4	XCVR_TX3_N	Gigabit Transceiver	T21	XCVR_0_TX3_N		
5	ETH_TXA_P	Ethernet Signal				ETH_TXA_P	6	XCVR_TX3_P	Gigabit Transceiver	T22	XCVR_0_TX3_P		
7	ETH_TXA_N	Ethernet Signal				ETH_TXA_N	8	GND					
9	GND						10	XCVR_RX3_N	Gigabit Transceiver	R19	XCVR_0_RX3_N		
11	ETH_TXB_P	Ethernet Signal				ETH_TXB_P	12	XCVR_RX3_P	Gigabit Transceiver	R20	XCVR_0_RX3_P		
13	ETH_TXB_N	Ethernet Signal				ETH_TXB_N	14	GND					
15	GND						16	XCVR_TX2_N	Gigabit Transceiver	P21	XCVR_0_TX2_N		
17	ETH_TXC_P	Ethernet Signal				ETH_TXC_P	18	XCVR_TX2_P	Gigabit Transceiver	P22	XCVR_0_TX2_P		
19	ETH_TXC_N	Ethernet Signal				ETH_TXC_N	20	GND					
21	GND						22	XCVR_RX2_N	Gigabit Transceiver	M21	XCVR_0_RX2_N		
23	ETH_TXD_P	Ethernet Signal				ETH_TXD_P	24	XCVR_RX2_P	Gigabit Transceiver	M22	XCVR_0_RX2_P		
25	ETH_TXD_N	Ethernet Signal				ETH_TXD_N	26	GND					
27	GND						28	XCVR_TX1_N	Gigabit Transceiver	H21	XCVR_0_TX1_N		
29	ETH_LINK_ON	Ethernet Signal				ETH_LINK_ON	30	XCVR_TX1_P	Gigabit Transceiver	H22	XCVR_0_TX1_P		
31	ETH_ACTIVITY_B	Ethernet Signal				ETH_ACTIVITY_B	32	GND					
33	GND						34	XCVR_RX1_N	Gigabit Transceiver	K21	XCVR_0_RX1_N		
35	XCVR_REFCLK2_N	Gigabit Transceiver	J20	XCVR_0C_REFCLK_N		XCVR_REFCLK2_N	36	XCVR_RX1_P	Gigabit Transceiver	K22	XCVR_0_RX1_P		
37	XCVR_REFCLK2_P	Gigabit Transceiver	J19	XCVR_0C_REFCLK_P		XCVR_REFCLK2_P	38	GND					
39	GND						40	XCVR_TX0_N	Gigabit Transceiver	F21	XCVR_0_TX0_N		

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
41	XCVR_REFCLK1_N	Gigabit Transceiver	L20	XCVR_0A_REFCLK_N		XCVR_REFCLK1_N	42	XCVR_TX0_P	Gigabit Transceiver	F22	XCVR_0_TX0_P		
43	XCVR_REFCLK1_P	Gigabit Transceiver	L19	XCVR_0A_REFCLK_P		XCVR_REFCLK1_P	44	GND					
45	GND						46	XCVR_RX0_N	Gigabit Transceiver	G19	XCVR_0_RX0_N		
47	XCVR_REFCLK0_N	Gigabit Transceiver	N20	XCVR_0B_REFCLK_N		XCVR_REFCLK0_N	48	XCVR_RX0_P	Gigabit Transceiver	G20	XCVR_0_RX0_P		
49	XCVR_REFCLK0_P	Gigabit Transceiver	N19	XCVR_0B_REFCLK_P		XCVR_REFCLK0_P	50	GND					
51	GND						52	SGMII_RX0_N	SGMII ETH 0		MSS_SGMII_RXN0		
53	OTG_D_N	Usb Signal				OTG_D_N	54	SGMII_RX0_P	SGMII ETH 0		MSS_SGMII_RXP0		
55	OTG_D_P	Usb Signal				OTG_D_P	56	SGMII_TX0_N	SGMII ETH 0		MSS_SGMII_TXN0		
57	GND						58	SGMII_TX0_P	SGMII ETH 0		MSS_SGMII_TXP0		
59	OTG_VBUS	Usb Signal				OTG_VBUS	60	GND					
61	OTG_CPEN	Usb Signal				OTG_CPEN	62	SGMII_RX1_N	SGMII ETH 1		MSS_SGMII_RXN1		
63	OTG_ID	Usb Signal				OTG_ID	64	SGMII_RX1_P	SGMII ETH 1		MSS_SGMII_RXP1		
65	-						66	SGMII_TX1_N	SGMII ETH 1		MSS_SGMII_TXN1		
67	-						68	SGMII_TX1_P	SGMII ETH 1		MSS_SGMII_TXP1		
69	GND						70	GND					
71	-						72						
73	-						74						
75	-						76						
77	-						78						
79	+1V8_VDD						80	+1V8_VDD					
81	BANK0_LVDS_0_P	FPGA Gpio	AA12	HSIO70PB0	1.8V		82	BANK0_LVDS_12_P	FPGA Gpio	W12	HSIO74PB0/CLKIN_N_2/CC C_NW_CLKIN_N_2/CCC_N W_PLL1_OUT0	1.8V	
83	BANK0_LVDS_0_N	FPGA Gpio	AB12	HSIO70NB0	1.8V		84	BANK0_LVDS_12_N	FPGA Gpio	V12	HSIO74NB0	1.8V	
85	BANK0_LVDS_1_P	FPGA Gpio	W13	HSIO71PB0	1.8V		86	BANK0_LVDS_13_P	FPGA Gpio	U14	HSIO75PB0/DQS/CCC_NW _PLL1_OUT0	1.8V	
87	BANK0_LVDS_1_N	FPGA Gpio	Y13	HSIO71NB0	1.8V		88	BANK0_LVDS_13_N	FPGA Gpio	U13	HSIO75NB0/DQS	1.8V	

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
89	BANK0_LVDS_2_P	FPGA Gpio	W19	HSIO61PB0	1.8V		90	BANK0_LVDS_14_P	FPGA Gpio	V14	HSIO72PB0/CLKIN_N_3/CC C_NW_CLKIN_N_3	1.8V	
91	BANK0_LVDS_2_N	FPGA Gpio	W18	HSIO61NB0	1.8V		92	BANK0_LVDS_14_N	FPGA Gpio	V15	HSIO72NB0	1.8V	
93	BANK0_LVDS_3_P	FPGA Gpio	AB18	HSIO60PB0/CLKIN_N_7	1.8V		94	BANK0_LVDS_15_P	FPGA Gpio	U15	HSIO73PB0/CCC_NW_PLL1 _OUT1	1.8V	
95	BANK0_LVDS_3_N	FPGA Gpio	AA18	HSIO60NB0	1.8V		96	BANK0_LVDS_15_N	FPGA Gpio	T15	HSIO73NB0	1.8V	
97	GND						98	GND					
99	BANK0_LVDS_4_P	FPGA Gpio	AB19	HSIO52PB0	1.8V		100	BANK0_LVDS_16_P	FPGA Gpio	V17	HSIO58PB0	1.8V	
101	BANK0_LVDS_4_N	FPGA Gpio	AB20	HSIO52NB0	1.8V		102	BANK0_LVDS_16_N	FPGA Gpio	V16	HSIO58NB0	1.8V	
103	BANK0_LVDS_5_P	FPGA Gpio	AA21	HSIO51PB0/DQS/CCC _NE_PLL0_OUT0	1.8V		104	BANK0_LVDS_17_P	FPGA Gpio	T17	HSIO55PB0/CCC_NE_PLL1 _OUT1	1.8V	
105	BANK0_LVDS_5_N	FPGA Gpio	AA22	HSIO51NB0/DQS	1.8V		106	BANK0_LVDS_17_N	FPGA Gpio	U17	HSIO55NB0	1.8V	
107	BANK0_LVDS_6_P	FPGA Gpio	Y20	HSIO49PB0/CCC_NE_ PLL0_OUT1	1.8V		108	BANK0_LVDS_18_P	FPGA Gpio	AB21	HSIO53PB0	1.8V	
109	BANK0_LVDS_6_N	FPGA Gpio	Y21	HSIO50NB0	1.8V		110	BANK0_LVDS_18_N	FPGA Gpio	AA20	HSIO53NB0	1.8V	
111	BANK0_LVDS_7_P	FPGA Gpio	W21	HSIO50PB0/CCC_NE_ CLKIN_N_10/CCC_NE_ PLL0_OUT0	1.8V		112	BANK0_LVDS_19_P	FPGA Gpio	Y19	HSIO62PB0/CLKIN_N_6	1.8V	
113	BANK0_LVDS_7_N	FPGA Gpio	V21	HSIO50NB0	1.8V		114	BANK0_LVDS_19_N	FPGA Gpio	Y18	HSIO62NB0	1.8V	
115	GND						116	GND					
117	BANK0_LVDS_8_P	FPGA Gpio	V20	HSIO54PB0/CLKIN_N_9/CCC_NE_CLKIN_N_9	1.8V		118	BANK0_LVDS_20_P	FPGA Gpio	W22	HSIO48PB0/CCC_NE_CLKI N_N_11	1.8V	
119	BANK0_LVDS_8_N	FPGA Gpio	V19	HSIO54NB0	1.8V		120	BANK0_LVDS_20_N	FPGA Gpio	V22	HSIO48NB0	1.8V	
121	BANK0_LVDS_9_P	FPGA Gpio	U18	HSIO56NB0	1.8V		122	BANK0_LVDS_21_N	FPGA Gpio	T13	HSIO77NB0	1.8V	
123	BANK0_LVDS_9_N	FPGA Gpio	U19	HSIO56PB0/CLKIN_N_8/CCC_NE_CLKIN_N_8 /CCC_NE_PLL1_OUT0	1.8V		124	BANK0_LVDS_21_P	FPGA Gpio	R12	HSIO77PB0/CCC_NW_CLKI N_N_0	1.8V	
125	BANK0_LVDS_10_P	FPGA Gpio	U12	HSIO76PB0/CCC_NW_ CLKIN_N_1	1.8V		126	BANK0_LVDS_22_N	FPGA Gpio	R16	HSIO57NB0/DQS	1.8V	
127	BANK0_LVDS_10_N	FPGA Gpio	T12	HSIO76NB0	1.8V		128	BANK0_LVDS_22_P	FPGA Gpio	T16	HSIO57PB0/DQS/CCC_NE_ PLL1_OUT0	1.8V	
129	BANK0_LVDS_11_P	FPGA Gpio	R15	HSIO59PB0	1.8V		130	-					

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
131	BANK0_LVDS_11_N	FPGA Gpio	R14	HSIO59NB0	1.8V		132	-					
133	GND						134	GND					
135	-						136	-					
137	-						138	-					
139	-						140	-					
141	-						142	-					
143	+VCCO_BANK1						144	+VCCAUX_BANK1					+3V3_ADJ
145	BANK1_LVDS_0_P	FPGA Gpio	G13	GPIO137PB1	+VCCO_B ANK1		146	BANK1_LVDS_14_P	FPGA Gpio	F17	GPIO11PB1/CLKIN_S_9/CC C_SE_CLKIN_S_9	+VCCO_B ANK1	LED1
147	BANK1_LVDS_0_N	FPGA Gpio	H13	GPIO137NB1	+VCCO_B ANK1		148	BANK1_LVDS_14_N	FPGA Gpio	F16	GPIO11NB1	+VCCO_B ANK1	LED2
149	BANK1_LVDS_1_P	FPGA Gpio	F12	GPIO133PB1	+VCCO_B ANK1		150	BANK1_LVDS_15_P	FPGA Gpio	E15	GPIO9PB1/CLKIN_S_8/CCC _SE_CLKIN_S_8/CCC_SE_P LL0_OUT0	+VCCO_B ANK1	LED3
151	BANK1_LVDS_1_N	FPGA Gpio	F11	GPIO133NB1	+VCCO_B ANK1		152	BANK1_LVDS_15_N	FPGA Gpio	E14	GPIO9NB1	+VCCO_B ANK1	LED4
153	BANK1_LVDS_2_P	FPGA Gpio	D12	GPIO135PB1	+VCCO_B ANK1		154	BANK1_LVDS_16_P	FPGA Gpio	C14	GPIO4PB1/LPRB_A	+VCCO_B ANK1	LED5
155	BANK1_LVDS_2_N	FPGA Gpio	E11	GPIO135NB1	+VCCO_B ANK1		156	BANK1_LVDS_16_N	FPGA Gpio	C15	GPIO4NB1/LPRB_B	+VCCO_B ANK1	LED6
157	BANK1_LVDS_3_P	FPGA Gpio	C19	GPIO18PB9	+VCCO_B ANK1		158	BANK1_LVDS_17_P	FPGA Gpio	A15	GPIO5PB1/CLKIN_S_7	+VCCO_B ANK1	LED7
159	BANK1_LVDS_3_N	FPGA Gpio	C20	GPIO18NB9	+VCCO_B ANK1		160	BANK1_LVDS_17_N	FPGA Gpio	B15	GPIO5NB1	+VCCO_B ANK1	LED8
161	GND						162	GND					
163	BANK1_LVDS_4_P	FPGA Gpio	E19	GPIO14PB1/DQS/CCC _SE_PLL1_OUT0	+VCCO_B ANK1		164	BANK1_LVDS_18_P	FPGA Gpio	C5	GPIO122PB1/DQS/CCC_S W_PLL1_OUT0	+VCCO_B ANK1	USER_BTN 1
165	BANK1_LVDS_4_N	FPGA Gpio	D19	GPIO14NB1/DQS	+VCCO_B ANK1		166	BANK1_LVDS_18_N	FPGA Gpio	B5	GPIO122NB1/DQS	+VCCO_B ANK1	USER_BTN 2
167	BANK1_LVDS_5_P	FPGA Gpio	D18	GPIO16PB1/CCC_SE_P LL1_OUT1	+VCCO_B ANK1		168	BANK1_LVDS_19_P	FPGA Gpio	A13	GPIO1PB1/CLKIN_S_5	+VCCO_B ANK1	USER_BTN 3
169	BANK1_LVDS_5_N	FPGA Gpio	E18	GPIO16NB1	+VCCO_B ANK1		170	BANK1_LVDS_19_N	FPGA Gpio	A12	GPIO1NB1	+VCCO_B ANK1	USER_BTN 4

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
171	BANK1_LVDS_6_P	FPGA Gpio	A18	GPIO17PB1/CCC_SE_C LKIN_S_11	+VCCO_B ANK1		172	BANK1_LVDS_20_P	FPGA Gpio	C11	GPIO130PB1/CCC_SW_PLL 0_OUT1	+VCCO_B ANK1	UART1_RX D
173	BANK1_LVDS_6_N	FPGA Gpio	B18	GPIO17NB1	+VCCO_B ANK1		174	BANK1_LVDS_20_N	FPGA Gpio	D11	GPIO130NB1	+VCCO_B ANK1	UART1_TX D
175	BANK1_LVDS_7_P	FPGA Gpio	B17	GPIO15PB1/CCC_SE_C LKIN_S_10/CCC_SE_P LL1_OUT0	+VCCO_B ANK1		176	BANK1_LVDS_21_P	FPGA Gpio	D9	GPIO126PB1	+VCCO_B ANK1	UART2_RX D
177	BANK1_LVDS_7_N	FPGA Gpio	C17	GPIO15NB1	+VCCO_B ANK1		178	BANK1_LVDS_21_N	FPGA Gpio	D8	GPIO126NB1	+VCCO_B ANK1	UART2_TX D
179	GND						180	GND					
181	BANK1_LVDS_8_P	FPGA Gpio	D13	GPIO2PB1/DQS	+VCCO_B ANK1		182	BANK1_LVDS_22_P	FPGA Gpio	C10	GPIO128PB1/DQS/CCC_S W_PLL0_OUT0	+VCCO_B ANK1	
183	BANK1_LVDS_8_N	FPGA Gpio	D14	GPIO2NB1/DQS	+VCCO_B ANK1		184	BANK1_LVDS_22_N	FPGA Gpio	C9	GPIO128NB1/DQS	+VCCO_B ANK1	
185	BANK1_LVDS_9_P	FPGA Gpio	B13	GPIO3PB1/CLKIN_S_6	+VCCO_B ANK1		186	BANK1_LVDS_23_P	FPGA Gpio	A8	GPIO127PB1	+VCCO_B ANK1	
187	BANK1_LVDS_9_N	FPGA Gpio	B14	GPIO3NB1	+VCCO_B ANK1		188	BANK1_LVDS_23_N	FPGA Gpio	B8	GPIO127NB1	+VCCO_B ANK1	
189	BANK1_LVDS_10_P	FPGA Gpio	B12	GPIO0PB1/CLKIN_S_4	+VCCO_B ANK1		190	BANK1_LVDS_24_P	FPGA Gpio	D7	GPIO120PB1/CCC_SW_CLK IN_S_0	+VCCO_B ANK1	
191	BANK1_LVDS_10_N	FPGA Gpio	C12	GPIO0NB1	+VCCO_B ANK1		192	BANK1_LVDS_24_N	FPGA Gpio	D6	GPIO120NB1	+VCCO_B ANK1	
193	BANK1_LVDS_11_P	FPGA Gpio	A10	GPIO129PB1/CCC_SW _PLL0_OUT0	+VCCO_B ANK1		194	BANK1_LVDS_25_P	FPGA Gpio	C6	GPIO123PB1/CLKIN_S_2/C CC_SW_CLKIN_S_2/CCC_S W_PLL1_OUT0	+VCCO_B ANK1	
195	BANK1_LVDS_11_N	FPGA Gpio	A11	GPIO129NB1	+VCCO_B ANK1		196	BANK1_LVDS_25_N	FPGA Gpio	C7	GPIO123NB1	+VCCO_B ANK1	
197	GND						198	GND					
199	BANK1_LVDS_12_P	FPGA Gpio	B10	GPIO131PB1	+VCCO_B ANK1		200	BANK1_LVDS_26_P	FPGA Gpio	A6	GPIO124PB1/CCC_SW_PLL 1_OUT1	+VCCO_B ANK1	
201	BANK1_LVDS_12_N	FPGA Gpio	B9	GPIO131NB1	+VCCO_B ANK1		202	BANK1_LVDS_26_N	FPGA Gpio	A5	GPIO124NB1	+VCCO_B ANK1	
203	BANK1_LVDS_13_P	FPGA Gpio	A7	GPIO125PB1/CLKIN_S _3/CCC_SW_CLKIN_S_ 3	+VCCO_B ANK1		204	BANK1_LVDS_27_P	FPGA Gpio	C4	GPIO121PB1/CCC_SW_CLK IN_S_1	+VCCO_B ANK1	

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
205	BANK1_LVDS_13_N	FPGA Gpio	B7	GPIO125NB1	+VCCO_B ANK1		206	BANK1_LVDS_27_N	FPGA Gpio	B4	GPIO121NB1	+VCCO_B ANK1	
207	+1V8_VDD						208	+3V3_VDD					
209	-						210	UART0_RXD	Uart Interface	D3	MSSIO28B2		UART0_RX D
211	-						212	UART0_TXD	Uart Interface	C2	MSSIO29B2		UART0_TX D
213	SD_DATA2	Sd Card		MSSIO4B4		SD_DATA2	214	I2C1_SCL	I2C Interface	C1	MSSIO26B2		I2C1_SCL
215	SD_DATA3	Sd Card		MSSIO5B4		SD_DATA3	216	I2C1_SDA	I2C Interface	B1	MSSIO27B2		I2C1_SDA
217	SD_CMD	Sd Card		MSSIO1B4		SD_CMD	218	QSPI_CLK	QSPI Interface	E5	MSSIO30B2		QSPI_CLK
219	SD_CLK	Sd Card		MSSIO0B4		SD_CLK	220	QSPI_SS0/CAN0_TX	QSPI Interface	E4	MSSIO31B2		QSPI_SS0/ CAN0_TX
221	SD_DATA0	Sd Card		MSSIO2B4		SD_DATA0	222	QSPI_DATA0/CAN0_RX	QSPI Interface	B2	MSSIO32B2		QSPI_DATA 0/CAN0_RX
223	SD_DATA1	Sd Card		MSSIO3B4		SD_DATA1	224	QSPI_DATA1	QSPI Interface	A2	MSSIO33B2		QSPI_DATA 1
225	SD_Wpn	Sd Card		MSSIO7B4		SD_Wpn	226	QSPI_DATA2/CAN1_TX	QSPI Interface	B3	MSSIO34B2		QSPI_DATA 2/CAN1_TX
227	SD_Cdn	Sd Card		MSSIO6B4		SD_Cdn	228	QSPI_DATA3/CAN1_RX	QSPI Interface	A3	MSSIO35B2		QSPI_DATA 3/CAN1_RX
229	GND						230	GND					
231	JTAG_TCK	Jtag Managing				JTAG_TCK	232	+3V3_VDD					
233	JTAG_TMS	Jtag Managing				JTAG_TMS	234	IO_CFG_INTF		H9	IO_CFG_INTF		IO_CFG_IN TF
235	JTAG_TDI	Jtag Managing				JTAG_TDI	236	SPI_EN	SPI Interface	H11	SPI_EN		SPI_EN
237	JTAG_TDO	Jtag Managing				JTAG_TDO	238	-					
239	JTAG_RSTn	Jtag Managing				JTAG_RSTn	240	SPI_CSN	SPI Interface	G7	SS		SPI_CSN
241	GND						242	SPI_SCLK	SPI Interface	E6	SCK		SPI_SCLK
243	SOM_PWR_EN	Power Managing				SOM_PWR_EN	244	SPI_MOSI	SPI Interface	F7	SDO		SPI_MOSI
245	SOM_PWR_BTN	Power Managing				SOM_PWR_BTN	246	SPI_MISO	SPI Interface	H10	SDI		SPI_MISO
247	SOM_PWR_OK	Power Managing				SOM_PWR_OK	248	-					
249	SOM_RSTn	Power Managing				SOM_RSTn	250	MCU_RSTn	Ctrl Crypto Interface				MCU_RSTn

Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name	Pin	Pin Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
251	+5V_BOARD	Power Input					252	SWDIO	Ctrl Crypto Interface				SWDIO
253	+5V_BOARD	Power Input					254	SWCLK	Ctrl Crypto Interface				SWCLK
255	+5V_BOARD	Power Input					256	MCU_UART_TX	Uart Crypto Interface				MCU_UART_TX
257	+5V_BOARD	Power Input					258	MCU_UART_RX	Uart Crypto Interface				MCU_UART_RX
259	+5V_BOARD	Power Input					260	+3V3_SYS					

CHAPTER 4

4. POWER SUPPLY

Section includes :

- **Power signals**
- **Power managing signals**

4.1 POWER SIGNALS

Read carefully the related sections before starting your power stage design. This module needs to be supplied up to +5V_{in} power. Refer to the table below for the power supply range specification.

Note: the system must provide at least a power of 2A at 5V to allow the start of the module.

	Min	Typ	Max
Voltage range	+4,9V	+5V	+5,25V
Module Current working mode	-	tbd mA	-
Module Current in standby mode		tbd mA	

Note: the measures in the table above are to be considered referred to the module with only the Linux OS running once loaded (during the OS transient load can reach also 600 mA), the use of graphic accelerators or other multimedia applications could be cause of higher consumption than those indicated.

In the following table is shown the module power supply pins' numbering, connect all power supply pins in order to avoid damage.

Odd Pin	Name	Primary Function Description	Even Pin	Name	Primary Function Description
3	GND	Power return-Ground reference	2	GND	Power return-Ground reference
9	GND	Power return-Ground reference	8	GND	Power return-Ground reference
15	GND	Power return-Ground reference	14	GND	Power return-Ground reference
21	GND	Power return-Ground reference	20	GND	Power return-Ground reference
27	GND	Power return-Ground reference	26	GND	Power return-Ground reference
33	GND	Power return-Ground reference	32	GND	Power return-Ground reference
39	GND	Power return-Ground reference	38	GND	Power return-Ground reference
45	GND	Power return-Ground reference	44	GND	Power return-Ground reference
51	GND	Power return-Ground reference	50	GND	Power return-Ground reference
57	GND	Power return-Ground reference	60	GND	Power return-Ground reference
69	GND	Power return-Ground reference	70	GND	Power return-Ground reference
79	+1V8_VDD	Power signal	80	+1V8_VDD	Power signal
97	GND	Power return-Ground reference	98	GND	Power return-Ground reference
115	GND	Power return-Ground reference	116	GND	Power return-Ground reference
133	GND	Power return-Ground reference	134	GND	Power return-Ground reference
143	+VCCO_1	Power signal	144	+VCCAUX_BANK1	Power signal

Odd Pin	Name	Primary Function Description	Even Pin	Name	Primary Function Description
161	GND	Power return-Ground reference	162	GND	Power return-Ground reference
179	GND	Power return-Ground reference	180	GND	Power return-Ground reference
197	GND	Power return-Ground reference	198	GND	Power return-Ground reference
207	+1V8_VDD	Power signal	208	+3V3_VDD	Power signal
229	GND	Power return-Ground reference	230	GND	Power return-Ground reference
241	GND	Power return-Ground reference	232	+3V3_VDD	Power signal
251	+5V_BOARD	Power input	260	+3V3_SYS	Power signal
253	+5V_BOARD	Power input			
255	+5V_BOARD	Power input			
257	+5V_BOARD	Power input			
259	+5V_BOARD	Power input			

4.2 POWER MANAGING SIGNALS

Following is shown power managing signals.

PIN	NAME	DVK NAME	DIRECTION	RAIL	Function Description
243	SOM_PWR_EN	SOM_PWR_EN	IN	+3.3V/+5V	Carrier power enable to module
245	SOM_PWR_BTN	SOM_PWR_BTN	IN	+3.3V/+5V	Carrier power button Not implemented by default
247	SOM_PWR_OK	SOM_PWR_OK	OUT	Output OD	Power good indication to carrier
249	SOM_RSTn	SOM_RSTn	IN	+3.3V	Drive low to reset SOM

Warning: Use SOM_PWR_OK to enable power to +VCCO_BANK1.

If +VCCO_BANK1 is active before SOM_PWR_OK FPGA can be damaged.

The right power sequence to the SOM is:

- Powering 5V to SOM,
- Use SOM_PWR_OK to enable all other baseboard power supply.

CHAPTER 5

5. INTERFACES

Section includes :

- Ethernet
- USB
- JTAG
- SPI
- SERIALS
- I2C
- GPIO

Warning! The schematics in chapters below are generic, please refer to the signals in the table.

5.1 ETHERNET

Kynesis Module supports one RGMII Gigabit Ethernet PHY connected to FPGA fabric and two SGMII ethernet.

In the following table are listed the MDI pin assignment on the SOM module connector for the RGMII PHY mounted on board

PIN	NAME	DVK NAME	NOTE
5	ETH_TXA_P	ETH_TXA_P	Diff100
7	ETH_TXA_N	ETH_TXA_N	
11	ETH_TXB_P	ETH_TXB_P	Diff100
13	ETH_TXB_N	ETH_TXB_N	
17	ETH_TXC_P	ETH_TXC_P	Diff100
19	ETH_TXC_N	ETH_TXC_N	
23	ETH_TXD_P	ETH_TXD_P	Diff100
25	ETH_TXD_N	ETH_TXD_N	
29	ETH_LINK_ON	ETH_LINK_ON	Output OD (12mA)
31	ETH_ACTIVITY_B	ETH_ACTIVITY_B	Output OD (12mA)

Ethernet PHY signals are shown in the table below.

PIN	PHY NAME	DVK NAME	FPGA PIN	FPGA NAME
19	TXD0	GEM0_TXD0	W16	HSIO83PB0
20	TXD1	GEM0_TXD1	AA17	HSIO81NB0/DQS
21	TXD2	GEM0_TXD2	AB17	HSIO81PB0/DQS
22	TXD3	GEM0_TXD3	Y16	HSIO82NB0
24	GTX_CLK	GEM0_TXCLK	AA16	HSIO82PB0
25	TX_EN	GEM0_TXCTL	W17	HDIO83NB0
27	RXD3/MODE3	GEM0_RXD3	Y14	HSIO87PB0/DQS/CCC_NW_PLL0_UT0
28	RXD2/MODE2	GEM0_RXD2	W14	HSIO87NB0/DQS
31	RXD1/MODE1	GEM0_RXD1	AB13	HSIO86NB0
32	RXD0/MODE0	GEM0_RXD0	AA13	HSIO86PB0/CLKIN_N_4/CCC_NW_PLL0_OUT0
33	RX_DV/CLK125_EN	GEM0_RXCTL	AB15	HSIO84NB0
35	RX_CLK/PHYAD2	GEM0_RXCLK	AB14	HSIO84PB0/CLKIN_N_5
36	MDC	GEM0_MDC	Y15	HSIO85PB0/CCC_NW_PLL0_OUT1
37	MDIO	GEM0_MDIO	AA15	HSIO85NB0
38	INT_N		D4	MSS I037
42	PHY_RESET_N		H5	MSS I012

5.1.1 LAN IMPLEMENTATION GUIDELINES

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the Kynesis module.

It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests.

Even if a Kynesis module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care has to be taken to route the signals between the magnetics and Ethernet connector. If only Fast Ethernet (100Mbit/s) is required, some design cost may be saved by using only 10/100Base-TX magnetics.

The Ethernet MDI signals are analogue differential pair signals which need to be routed carefully.

Try to keep the MDI signals as short as possible and keep them away from digital signals. Try to avoid any stubs on these signals.

If discrete magnetics are used instead of a RJ-45 Ethernet jack with integrated magnetics, special care has to be taken to route the signals between the magnetics and the jack. These signals are required to be high voltage isolated from the other signals. It is therefore necessary to place a dedicated ground plane under these signals which has a minimum separation of 2mm from every other signal and plane.

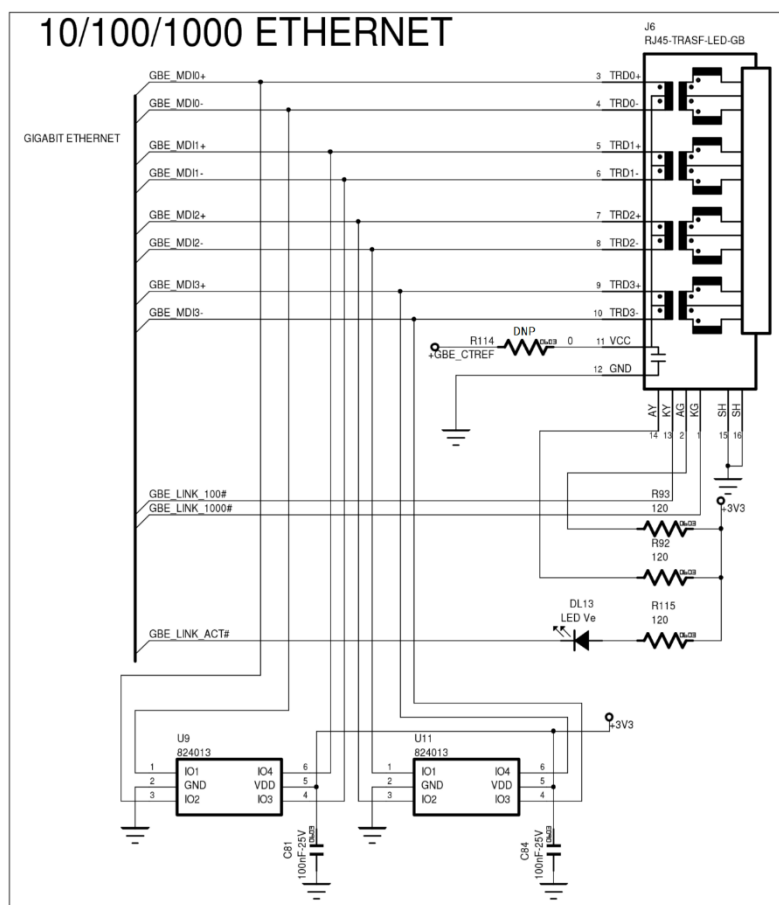
The use of dedicated suppressor is recommended in order to avoid PHY damage by fast high transient voltage peak.

The PHY used in the module is the **Microchip KSZ9031RNX**.

Refer to the **KSZ9031RNX-HW-Design-Checklist-00003391.pdf** for more information.

The need for centre tap voltage depends on the Ethernet PHY used on the Kynesis module.

The following figure shows a typical GBE connection.



Note: refer to the Gbit Ethernet specifications for further details about the board's design and the relative PCB master.

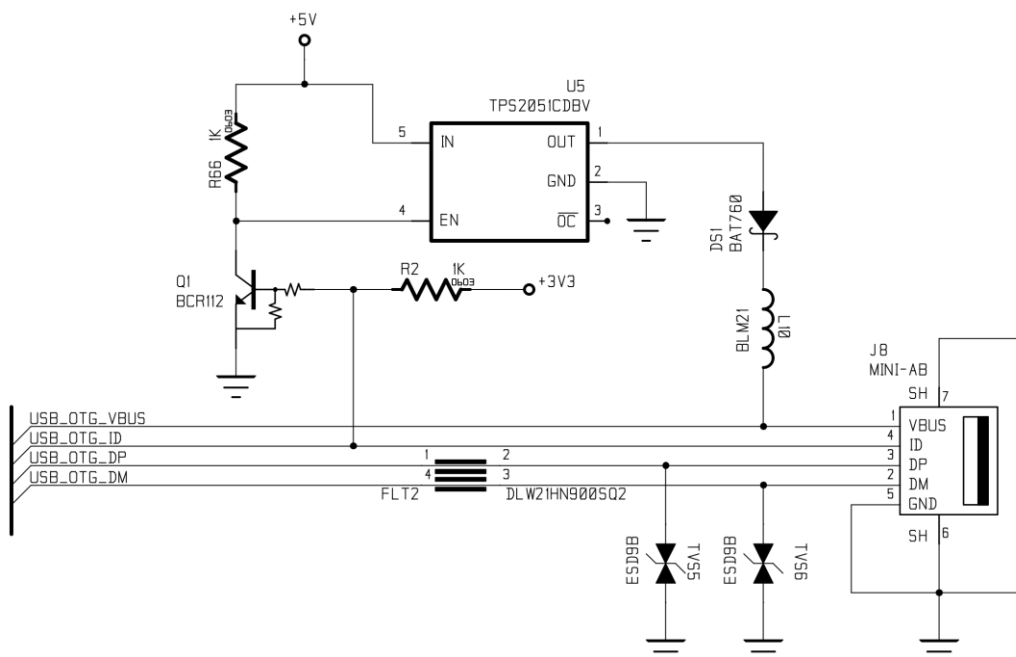
5.2 USB

Warning! The schematics in chapters below are generic, please refer to the signals in the table.

5.2.1 USB OTG

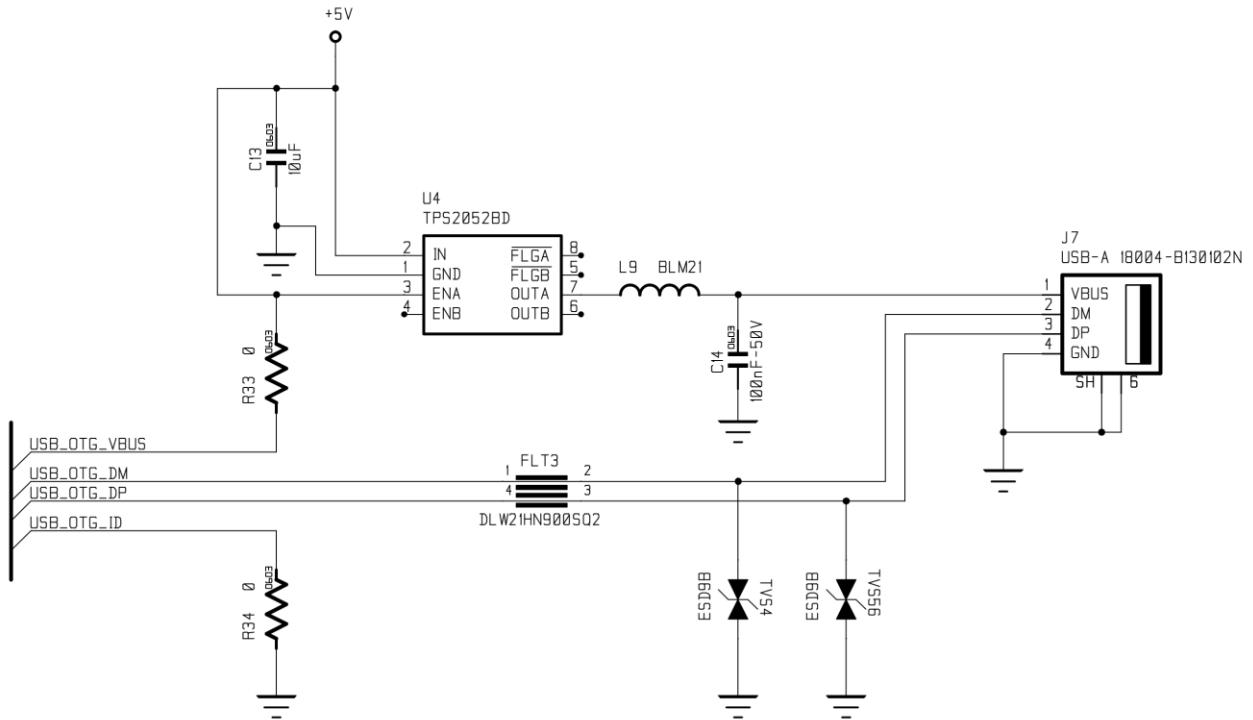
The Microchip® Kynesis USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. The figure shows how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. The following table lists all USB/OTG signal of main connector.

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

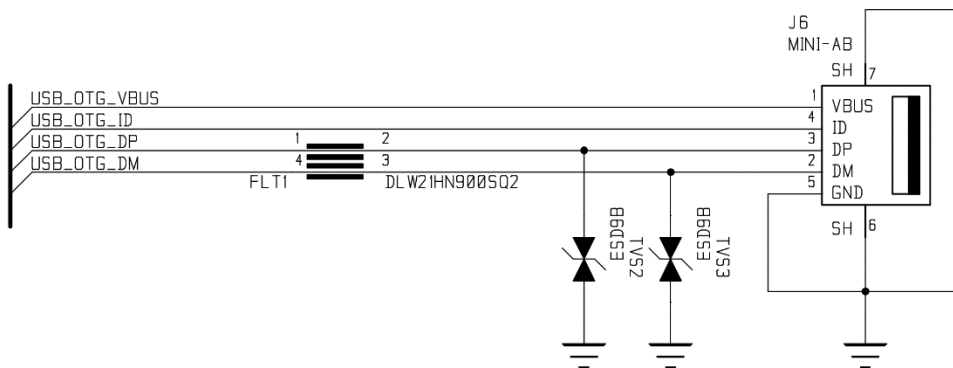


PIN	NAME	DVK NAME	GPIO CAPABLE	RAIL	Primary function description
53	OTG_D_N	OTG_D_N	N	-	USB on the go interface
55	OTG_D_P	OTG_D_P	N	-	USB on the go interface
59	OTG_VBUS	OTG_VBUS	N	5V	USB on the go interface
61	OTG_CPEN	OTG_CPEN	N	-	USB on the go interface
63	OTG_ID	OTG_ID	N	-	USB on the go interface

Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND



Use of the USB OTG port as Device.



5.3 MSS IO ASSIGNMENT

On the Polarfire architecture RISC-V peripheral can be assigned to MSS IO PIN or redirected to FPGA Fabric. In the following table is shown the assignment of the pin on the SOM. Pins highlighted in green are connected to specific hardware on the SOM and must not be changed. Refer to Microchip pfsoc_mss_configurator_ug.pdf for configuration setting.

It is important to use the preset available from Enktron GIT

BANK	MSS PIN	PIN	PRIMARY SOM FUNCTION	FUNCTION 1	FUNCTION 2	FUNCTION 3	FUNCTION 4	DESCRIPTION	
BANK	0	J1	EMMC_CLK	SD_CLK				eMMC or SDCARD connection	
	1	K5	EMMC_CMD	SD_CMD					
	2	H1	EMMC_DATA0	SD_DATA0					
	3	J4	EMMC_DATA1	SD_DATA1					
	4	K4	EMMC_DATA2	SD_DATA2					
	5	J7	EMMC_DATA3	SD_DATA3					
	6	K3	EMMC_STRB	SD_CD					
	7	H4	EMMC_RSTN	SD_WP					
	8								
			J6	EMMC_DATA4					
	9	H6	EMMC_DATA5						
	10	J3	EMMC_DATA6						
	11	H2	EMMC_DATA7						
12	H5	GPIO_0_12					Ethernet Reset active low pin		
13	J2	GPIO_0_13					eMMC/SDCARD Mux control 0: eMMC 1: SDCARD		
BANK	14	G2	USB_CLK					USB PHY connection	
	15	F1	USB_DIR						
	16	G5	USB_NXT						
	17	G4	USB_STP						
	18	F2	USB_DATA0						
	19	E1	USB_DATA1						
	20	G3	USB_DATA2						
	21	F5	USB_DATA3						
	22	D1	USB_DATA4						
	23	D2	USB_DATA5						
	24	F6	USB_DATA6						
	25	F3	USB_DATA7						
	26	C1	I2C_1_SCL (B)						
	27	B1	I2C_1_SDA (B)						
	28	D3	MMUART_0_RXD (B)						
	29	C2	MMUART_0_TXD (B)						
30	E5		QSPI_CLK (B)	SPI_1_CLK (B)	CAN_0_TXBUS (B)	GPIO_1_16	Generic Pin, no function implemented on SOM, connected directly to SOM		
31	E4		QSPI_SS0	SPI_1_SS0 (B)	CAN_0_RXBUS (B)	GPIO_1_17			
32	B2		QSPI_DATA0	SPI_1_DO (B)	CAN_0_TX_EBLN (B)	GPIO_1_18			
33	A2		QSPI_DATA1	SPI_1_DI (B)	CAN_1_TXBUS (B)	GPIO_1_19			

BANK	MSS PIN	PIN	PRIMARY SOM FUNCTION	FUNCTION 1	FUNCTION 2	FUNCTION 3	FUNCTION 4	DESCRIPTION
	34	B3		QSPI_DATA2		CAN_1_RXBUS (B)	GPIO_1_20	
	35	A3		QSPI_DATA3			GPIO_1_21	
	36	E3	GPIO_1_22					USB PHY reset active low
	37	D4	GPIO_1_23					Ethernet PHY interrupt active low

Note: BANK4 signals are powered from 1.8V and BANK2 signal are powered from 3.3V.

5.4 MSS UARTS

Polarfire has 5 UARTs; in the Kynesis module one UART interface is assigned directly to MSS IO Pin. Other serials can be assigned to FPGA pin.

The signals on the module's UART pins are 3.3V logic level, this cannot be connected directly to a RS232 device like a PC Serial port, the use of a transceiver on the base board is mandatory in order to avoid module damage.

The following table describes the specifications of the interface

Pin	Name	Primary function	FPGA Pin	FPGA Name	Rail	DVK Name
210	UART0_RXD	Uart Interface	D3	MSSIO28B2		UART0_RXD
212	UART0_TXD	Uart Interface	C2	MSSIO29B2		UART0_TXD

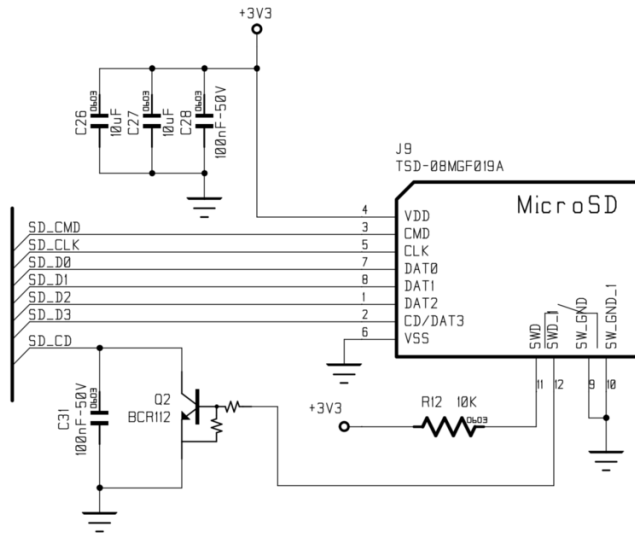
5.5 SD CARD/EMMC MULTIPLEXING

In the SOM, eMMC and SDCARD share the same pins on MSS IO. In SOM board eMMC and SDCARD share the same pin on MSS IO. A hardware multiplexer is implemented to select between the two peripherals

MSS Pin	Pin	Primary SOM function	Function 2
0	J1	EMMC_CLK	SD_CLK
1	K5	EMMC_CMD	SD_CMD
2	H1	EMMC_DATA0	SD_DATA0
3	J4	EMMC_DATA1	SD_DATA1
4	K4	EMMC_DATA2	SD_DATA2
5	J7	EMMC_DATA3	SD_DATA3
6	K3	EMMC_STRB	SD_CD
7	H4	EMMC_RSTN	SD_WP
8	J6	EMMC_DATA4	
9	H6	EMMC_DATA5	
10	J3	EMMC_DATA6	
11	H2	EMMC_DATA7	
12	J2	GPIO_0_13	

GPIO_0_13 controls the multiplexer switching. Set to 0 to select eMMC, set to 1 to select SDCARD

The Microchip® Kynesis Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module includes these features and the figure shows how the Micro SD Card connector is connected to Kynesis Module in the evaluation board. The uSDHC signal of the module's main connector are listed in table below.



Pin	Name	Primary function	MSSIO Name	GPIO Capable	DVK Name
213	SD_DATA2	Sd Card	MSSIO4	N	SD_DATA2
215	SD_DATA3	Sd Card	MSSIO5	N	SD_DATA3
217	SD_CMD	Sd Card	MSSIO1	N	SD_CMD
219	SD_CLK	Sd Card	MSSIO0	N	SD_CLK
221	SD_DATA0	Sd Card	MSSIO2	N	SD_DATA0
223	SD_DATA1	Sd Card	MSSIO3	N	SD_DATA1
225	SD_Wpn	Sd Card	MSSIO7	N	SD_Wpn
227	SD_Cdn	Sd Card	MSSIO6	N	SD_Cdn

5.6 MSS GPIO

The following MSS IO pin are used as GPIO with assigned function on the SOM and must not be changed

Pin Name	Pin Loc	Name	Direction	Description
MSSIO12	H5	GPIO_0_12	OUT	Ethernet PHY active low reset pin
MSSIO13	J2	GPIO_0_13	OUT	eMMC/SDCARD Mux control 0: eMMC 1: SDCARD
MSSIO36	E3	GPIO_1_22	OUT	USB PHY active low reset pin
MSSIO37	D4	GPIO_1_23	INPUT	Ethernet PHY active low interrupt

The following MSS IO pin are connected directly to SOM pin and the user can assign the preferred function

MSSIO Pin	Pin Loc	QSPI	SPI	CAN	GPIO
MSSIO30	E5	QSPI_CLK (B)	SPI_1_CLK (B)	CAN_0_TXBUS (B)	GPIO_1_16
MSSIO31	E4	QSPI_SS0	SPI_1_SS0 (B)	CAN_0_RXBUS (B)	GPIO_1_17
MSSIO32	B2	QSPI_DATA0	SPI_1_DO (B)	CAN_0_TX_EBL_N (B)	GPIO_1_18
MSSIO33	A2	QSPI_DATA1	SPI_1_DI (B)	CAN_1_TXBUS (B)	GPIO_1_19
MSSIO34	B3	QSPI_DATA2		CAN_1_RXBUS (B)	GPIO_1_20
MSSIO35	A3	QSPI_DATA3			GPIO_1_21

5.7 MSS I2C

An I2C interface is connected to MSS IO pin. There is also present another I2C interface that can be routed to FPGA fabric pin

Pin	Name	Primary function	FPGA Pin	FPGA Name	Rail	DVK Name
214	I2C1_SCL	I2C Interface	C1	MSSIO26		I2C1_SCL
216	I2C1_SDA	I2C Interface	B1	MSSIO27		I2C1_SDA

5.8 JTAG

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan. JTAG is often used as an IC debug or probing port.

Pin	Name	Primary function	FPGA Pin	FPGA Name	Voltage	DVK Name
231	JTAG_TCK	Jtag Managing				JTAG_TCK
233	JTAG_TMS	Jtag Managing				JTAG_TMS
235	JTAG_TDI	Jtag Managing				JTAG_TDI
237	JTAG_TDO	Jtag Managing				JTAG_TDO
239	JTAG_RSTn	Jtag Managing				JTAG_RSTn

5.9 FPGA FABRIC GPIO

The following FPGA Fabric pins are allocated as general-purpose IO, they have all bidirectional capability but also a preferred direction.

Pin	Name	Primary funcion	FPGA Pin	FPGA Name	Rail	DVK Name
81	BANK0_LVDS_0_P	FPGA Gpio	AA12	HSIO70PB0	1.8V	
83	BANK0_LVDS_0_N	FPGA Gpio	AB12	HSIO70NB0	1.8V	
85	BANK0_LVDS_1_P	FPGA Gpio	W13	HSIO71PB0	1.8V	
87	BANK0_LVDS_1_N	FPGA Gpio	Y13	HSIO71NB0	1.8V	
89	BANK0_LVDS_2_P	FPGA Gpio	W19	HSIO61PB0	1.8V	
91	BANK0_LVDS_2_N	FPGA Gpio	W18	HSIO61NB0	1.8V	
82	BANK0_LVDS_12_P	FPGA Gpio	W12	HSIO74PB0/CLKIN_N_2/CCC_NW_CLKI N_N_2/CCC_NW_PL L1_OUT0	1.8V	
84	BANK0_LVDS_12_N	FPGA Gpio	V12	HSIO74NB0	1.8V	
86	BANK0_LVDS_13_P	FPGA Gpio	U14	HSIO75PB0/DQS/CC_NW_PLL1_OUT0	1.8V	

Pin	Name	Primary funcion	FPGA Pin	FPGA Name	Rail	DVK Name
88	BANK0_LVDS_13_N	FPGA Gpio	U13	HSIO75NB0/DQS	1.8V	
90	BANK0_LVDS_14_P	FPGA Gpio	V14	HSIO72PB0/CLKIN_N_3/CCC_NW_CLKI N_N_3	1.8V	
92	BANK0_LVDS_14_N	FPGA Gpio	V15	HSIO72NB0	1.8V	
93	BANK0_LVDS_3_P	FPGA Gpio	AB18	HSIO60PB0/CLKIN_N_7	1.8V	
95	BANK0_LVDS_3_N	FPGA Gpio	AA18	HSIO60NB0	1.8V	
99	BANK0_LVDS_4_P	FPGA Gpio	AB19	HSIO52PB0	1.8V	
101	BANK0_LVDS_4_N	FPGA Gpio	AB20	HSIO52NB0	1.8V	
103	BANK0_LVDS_5_P	FPGA Gpio	AA21	HSIO51PB0/DQS/C CC_NE_PLL0_OUT0	1.8V	
105	BANK0_LVDS_5_N	FPGA Gpio	AA22	HSIO51NB0/DQS	1.8V	
107	BANK0_LVDS_6_P	FPGA Gpio	Y20	HSIO49PB0/CCC_N E_PLL0_OUT1	1.8V	
109	BANK0_LVDS_6_N	FPGA Gpio	Y21	HSIO50NB0	1.8V	
111	BANK0_LVDS_7_P	FPGA Gpio	W21	HSIO50PB0/CCC_N E_CLKIN_N_10/CCC _NE_PLL0_OUT0	1.8V	
113	BANK0_LVDS_7_N	FPGA Gpio	V21	HSIO50NB0	1.8V	
117	BANK0_LVDS_8_P	FPGA Gpio	V20	HSIO54PB0/CLKIN_N_9/CCC_NE_CLKI N_N_9	1.8V	
119	BANK0_LVDS_8_N	FPGA Gpio	V19	HSIO54NB0	1.8V	
121	BANK0_LVDS_9_P	FPGA Gpio	U18	HSIO56NB0	1.8V	
123	BANK0_LVDS_9_N	FPGA Gpio	U19	HSIO56PB0/CLKIN_N_8/CCC_NE_CLKI N_N_8/CCC_NE_PL L1_OUT0	1.8V	
125	BANK0_LVDS_10_P	FPGA Gpio	U12	HSIO76PB0/CCC_N W_CLKIN_N_1	1.8V	
127	BANK0_LVDS_10_N	FPGA Gpio	T12	HSIO76NB0	1.8V	
94	BANK0_LVDS_15_P	FPGA Gpio	U15	HSIO73PB0/CCC_N W_PLL1_OUT1	1.8V	
96	BANK0_LVDS_15_N	FPGA Gpio	T15	HSIO73NB0	1.8V	
100	BANK0_LVDS_16_P	FPGA Gpio	V17	HSIO58PB0	1.8V	
102	BANK0_LVDS_16_N	FPGA Gpio	V16	HSIO58NB0	1.8V	
104	BANK0_LVDS_17_P	FPGA Gpio	T17	HSIO55PB0/CCC_N E_PLL1_OUT1	1.8V	
106	BANK0_LVDS_17_N	FPGA Gpio	U17	HSIO55NB0	1.8V	
108	BANK0_LVDS_18_P	FPGA Gpio	AB21	HSIO53PB0	1.8V	
110	BANK0_LVDS_18_N	FPGA Gpio	AA20	HSIO53NB0	1.8V	
112	BANK0_LVDS_19_P	FPGA Gpio	Y19	HSIO62PB0/CLKIN_N_6	1.8V	
114	BANK0_LVDS_19_N	FPGA Gpio	Y18	HSIO62NB0	1.8V	
118	BANK0_LVDS_20_P	FPGA Gpio	W22	HSIO48PB0/CCC_N E_CLKIN_N_11	1.8V	
120	BANK0_LVDS_20_N	FPGA Gpio	V22	HSIO48NB0	1.8V	

Pin	Name	Primary funcion	FPGA Pin	FPGA Name	Rail	DVK Name
122	BANK0_LVDS_21_N	FPGA Gpio	T13	HSIO77NB0	1.8V	
124	BANK0_LVDS_21_P	FPGA Gpio	R12	HSIO77PB0/CCC_N W_CLKIN_N_0	1.8V	
126	BANK0_LVDS_22_N	FPGA Gpio	R16	HSIO57NB0/DQS	1.8V	
128	BANK0_LVDS_22_P	FPGA Gpio	T16	HSIO57PB0/DQS/C CC_NE_PLL1_OUT0	1.8V	
129	BANK0_LVDS_11_P	FPGA Gpio	R15	HSIO59PB0	1.8V	
131	BANK0_LVDS_11_N	FPGA Gpio	R14	HSIO59NB0	1.8V	
145	BANK1_LVDS_0_P	FPGA Gpio	G13	GPIO137PB1	+VCCO_BANK1	
147	BANK1_LVDS_0_N	FPGA Gpio	H13	GPIO137NB1	+VCCO_BANK1	
149	BANK1_LVDS_1_P	FPGA Gpio	F12	GPIO133PB1	+VCCO_BANK1	
151	BANK1_LVDS_1_N	FPGA Gpio	F11	GPIO133NB1	+VCCO_BANK1	
153	BANK1_LVDS_2_P	FPGA Gpio	D12	GPIO135PB1	+VCCO_BANK1	
155	BANK1_LVDS_2_N	FPGA Gpio	E11	GPIO135NB1	+VCCO_BANK1	
157	BANK1_LVDS_3_P	FPGA Gpio	C19	GPIO18PB9	+VCCO_BANK1	
159	BANK1_LVDS_3_N	FPGA Gpio	C20	GPIO18NB9	+VCCO_BANK1	
163	BANK1_LVDS_4_P	FPGA Gpio	E19	GPIO14PB1/DQS/C CC_SE_PLL1_OUT0	+VCCO_BANK1	
165	BANK1_LVDS_4_N	FPGA Gpio	D19	GPIO14NB1/DQS	+VCCO_BANK1	
146	BANK1_LVDS_14_P	FPGA Gpio	F17	GPIO11PB1/CLKIN_ S_9/CCC_SE_CLKIN_ S_9	+VCCO_BANK1	LED1
148	BANK1_LVDS_14_N	FPGA Gpio	F16	GPIO11NB1	+VCCO_BANK1	LED2
150	BANK1_LVDS_15_P	FPGA Gpio	E15	GPIO9PB1/CLKIN_S _8/CCC_SE_CLKIN_ S_8/CCC_SE_PLL0_ OUT0	+VCCO_BANK1	LED3
152	BANK1_LVDS_15_N	FPGA Gpio	E14	GPIO9NB1	+VCCO_BANK1	LED4
154	BANK1_LVDS_16_P	FPGA Gpio	C14	GPIO4PB1/LPRB_A	+VCCO_BANK1	LED5
156	BANK1_LVDS_16_N	FPGA Gpio	C15	GPIO4NB1/LPRB_B	+VCCO_BANK1	LED6
158	BANK1_LVDS_17_P	FPGA Gpio	A15	GPIO5PB1/CLKIN_S _7	+VCCO_BANK1	LED7
160	BANK1_LVDS_17_N	FPGA Gpio	B15	GPIO5NB1	+VCCO_BANK1	LED8
164	BANK1_LVDS_18_P	FPGA Gpio	C5	GPIO122PB1/DQS/ CCC_SW_PLL1_OUT 0	+VCCO_BANK1	USER_BTN1
166	BANK1_LVDS_18_N	FPGA Gpio	B5	GPIO122NB1/DQS	+VCCO_BANK1	USER_BTN2
167	BANK1_LVDS_5_P	FPGA Gpio	D18	GPIO16PB1/CCC_S E_PLL1_OUT1	+VCCO_BANK1	
169	BANK1_LVDS_5_N	FPGA Gpio	E18	GPIO16NB1	+VCCO_BANK1	
171	BANK1_LVDS_6_P	FPGA Gpio	A18	GPIO17PB1/CCC_S E_CLKIN_S_11	+VCCO_BANK1	
173	BANK1_LVDS_6_N	FPGA Gpio	B18	GPIO17NB1	+VCCO_BANK1	
175	BANK1_LVDS_7_P	FPGA Gpio	B17	GPIO15PB1/CCC_S E_CLKIN_S_10/CCC _SE_PLL1_OUT0	+VCCO_BANK1	
177	BANK1_LVDS_7_N	FPGA Gpio	C17	GPIO15NB1	+VCCO_BANK1	

Pin	Name	Primary funcion	FPGA Pin	FPGA Name	Rail	DVK Name
181	BANK1_LVDS_8_P	FPGA Gpio	D13	GPIO2PB1/DQS	+VCCO_BANK1	
183	BANK1_LVDS_8_N	FPGA Gpio	D14	GPIO2NB1/DQS	+VCCO_BANK1	
185	BANK1_LVDS_9_P	FPGA Gpio	B13	GPIO3PB1/CLKIN_S_6	+VCCO_BANK1	
187	BANK1_LVDS_9_N	FPGA Gpio	B14	GPIO3NB1	+VCCO_BANK1	
189	BANK1_LVDS_10_P	FPGA Gpio	B12	GPIO0PB1/CLKIN_S_4	+VCCO_BANK1	
191	BANK1_LVDS_10_N	FPGA Gpio	C12	GPIO0NB1	+VCCO_BANK1	
193	BANK1_LVDS_11_P	FPGA Gpio	A10	GPIO129PB1/CCC_SW_PLL0_OUT0	+VCCO_BANK1	
195	BANK1_LVDS_11_N	FPGA Gpio	A11	GPIO129NB1	+VCCO_BANK1	
168	BANK1_LVDS_19_P	FPGA Gpio	A13	GPIO1PB1/CLKIN_S_5	+VCCO_BANK1	USER_BTN3
170	BANK1_LVDS_19_N	FPGA Gpio	A12	GPIO1NB1	+VCCO_BANK1	USER_BTN4
172	BANK1_LVDS_20_P	FPGA Gpio	C11	GPIO130PB1/CCC_SW_PLL0_OUT1	+VCCO_BANK1	UART1_RXD
174	BANK1_LVDS_20_N	FPGA Gpio	D11	GPIO130NB1	+VCCO_BANK1	UART1_TXD
176	BANK1_LVDS_21_P	FPGA Gpio	D9	GPIO126PB1	+VCCO_BANK1	UART2_RXD
178	BANK1_LVDS_21_N	FPGA Gpio	D8	GPIO126NB1	+VCCO_BANK1	UART2_TXD
182	BANK1_LVDS_22_P	FPGA Gpio	C10	GPIO128PB1/DQS/CCC_SW_PLL0_OUT0	+VCCO_BANK1	
184	BANK1_LVDS_22_N	FPGA Gpio	C9	GPIO128NB1/DQS	+VCCO_BANK1	
186	BANK1_LVDS_23_P	FPGA Gpio	A8	GPIO127PB1	+VCCO_BANK1	
188	BANK1_LVDS_23_N	FPGA Gpio	B8	GPIO127NB1	+VCCO_BANK1	
190	BANK1_LVDS_24_P	FPGA Gpio	D7	GPIO120PB1/CCC_SW_CLKIN_S_0	+VCCO_BANK1	
192	BANK1_LVDS_24_N	FPGA Gpio	D6	GPIO120NB1	+VCCO_BANK1	
194	BANK1_LVDS_25_P	FPGA Gpio	C6	GPIO123PB1/CLKIN_S_2/CCC_SW_CLKIN_S_2/CCC_SW_PL L1_OUT0	+VCCO_BANK1	
196	BANK1_LVDS_25_N	FPGA Gpio	C7	GPIO123NB1	+VCCO_BANK1	
199	BANK1_LVDS_12_P	FPGA Gpio	B10	GPIO131PB1	+VCCO_BANK1	
201	BANK1_LVDS_12_N	FPGA Gpio	B9	GPIO131NB1	+VCCO_BANK1	
203	BANK1_LVDS_13_P	FPGA Gpio	A7	GPIO125PB1/CLKIN_S_3/CCC_SW_CLKIN_S_3	+VCCO_BANK1	
205	BANK1_LVDS_13_N	FPGA Gpio	B7	GPIO125NB1	+VCCO_BANK1	
200	BANK1_LVDS_26_P	FPGA Gpio	A6	GPIO124PB1/CCC_SW_PLL1_OUT1	+VCCO_BANK1	
202	BANK1_LVDS_26_N	FPGA Gpio	A5	GPIO124NB1	+VCCO_BANK1	
204	BANK1_LVDS_27_P	FPGA Gpio	C4	GPIO121PB1/CCC_SW_CLKIN_S_1	+VCCO_BANK1	
206	BANK1_LVDS_27_N	FPGA Gpio	B4	GPIO121NB1	+VCCO_BANK1	

CHAPTER 6

6. PRODUCT COMPLIANCE

In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam in this chapter confirms the compliance, when applicable, of its own products to the normative ROHS and REACH and to the recognized hazards.

No hazard to report!

CHAPTER 7

7.ENGICAM INFORMATION

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7.2 SUPPORT

We offer an on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

ENGICAM Product Experts are available to answer questions via email:

7.3 CONTACT INFORMATION

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